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---

1 **Estimation of linear filter banks for multivariate time series prediction with temporal principal component analysis**
Van Veelen, M.; Nijhuis, J.A.G.; Spaanenburg, L.;
Neural Networks, 1999. IJCNN '99. International Joint Conference on , Volume: 4 , 10-16 July 1999
Pages:2624 - 2628 vol.4

[Abstract] [PDF Full-Text (436 KB)] IEEE CNF

---

2 **Comparative study of stock trend prediction using time delay, recurrent and probabilistic neural networks**
Saad, E.W.; Prokhorov, D.V.; Wunsch, D.C., II;
Neural Networks, IEEE Transactions on , Volume: 9 , Issue: 6 , Nov. 1998
Pages:1456 - 1470

[Abstract] [PDF Full-Text (396 KB)] IEEE JNL

---

3 **Advanced neural network training methods for low false alarm stock trend prediction**
Saad, E.W.; Prokhorov, D.V.; Wunsch, D.C.;
Neural Networks, 1996., IEEE International Conference on , Volume: 4 , 3-6 June 1996
Pages:2021 - 2026 vol.4

[Abstract] [PDF Full-Text (276 KB)] IEEE CNF

---

4 **A new automatic IIR analysis/synthesis technique for plucked-string instruments**
Su, A.W.Y.; Sheng-Fu Liang;
Speech and Audio Processing, IEEE Transactions on , Volume: 9 , Issue: 7 , Oct.

2001
Pages:747 - 754

[Abstract] [PDF Full-Text (192 KB)] IEEE JNL

---

5 **Extracting the relevant delays in time series modelling**
Goutte, C.;
Neural Networks for Signal Processing [1997] VII. Proceedings of the 1997 IEEE Workshop , 24-26 Sept. 1997
Pages:92 - 101

[Abstract] [PDF Full-Text (584 KB)] IEEE CNF

---

6 **Proceedings of 1994 33rd IEEE Conference on Decision and Control**

Decision and Control, 1994., Proceedings of the 33rd IEEE Conference on , Volume: 1 , 14-16 Dec. 1994
[Abstract] [PDF Full-Text (108 KB)] IEEE CNF

---

7 **Proceedings of 32nd IEEE Conference on Decision and Control**

Decision and Control, 1993., Proceedings of the 32nd IEEE Conference on , 15-17 Dec. 1993
[Abstract] [PDF Full-Text (20 KB)] IEEE CNF

---

8 **Neural networks based adaptive predictors for nonlinear dynamical systems**
Yongfeng Miao; Zhengmao Li;
Neural Networks, 1991. 1991 IEEE International Joint Conference on , 18-21 Nov. 1991
Pages:777 - 782 vol.1

[Abstract] [PDF Full-Text (268 KB)] IEEE CNF

---

9 **Adaptive PID control with neural network based predictor**
Yonghong Tan; De Keyser, R.;
Control, 1994. Control '94. Volume 2., International Conference on , 21-24 Mar 1994
Pages:1490 - 1494 vol.2

[Abstract] [PDF Full-Text (248 KB)] IEE CNF

---

10 **Nonlinear adaptive prediction of nonstationary signals**
Haykin, S.; Liang Li;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on] , Volume: 43 , Issue: 2 , Feb. 1995
Pages:526 - 535

[Abstract] [PDF Full-Text (740 KB)] IEEE JNL

---

11 **Nonlinear noise filtering and beamforming using the perceptron and its Volterra approximation**
Knecht, W.;

Speech and Audio Processing, IEEE Transactions on , Volume: 2 , Issue: 1 , Jan. 1994
Pages:55 - 62

[Abstract] [PDF Full-Text (712 KB)] IEEE JNL

---

12 **Back propagation through adjoints for the identification of nonlinear dynamic systems using recurrent neural models**
Srinivasan, B.; Prasad, U.R.; Rao, N.J.;
Neural Networks, IEEE Transactions on , Volume: 5 , Issue: 2 , March 1994
Pages:213 - 228

[Abstract] [PDF Full-Text (1328 KB)] IEEE JNL

---

13 **Continuous-time temporal back-propagation with adaptable time delays**
Day, S.P.; Davenport, M.R.;
Neural Networks, IEEE Transactions on , Volume: 4 , Issue: 2 , March 1993
Pages:348 - 354

[Abstract] [PDF Full-Text (572 KB)] IEEE JNL

---

14 **Proceedings of the 39th IEEE Conference on Decision and Control (Cat. No.00CH37187)**

Decision and Control, 2000. Proceedings of the 39th IEEE Conference on , Volume: 2 , 12-15 Dec. 2000
[Abstract] [PDF Full-Text (3668 KB)] IEEE CNF

---

15 **From adaptive linear to information filtering**
Principe, J.C.; Erdogmus, D.;
Adaptive Systems for Signal Processing, Communications, and Control Symposium 2000. AS-SPCC. The IEEE 2000 , 1-4 Oct. 2000
Pages:99 - 104

[Abstract] [PDF Full-Text (436 KB)] IEEE CNF

---

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---

16 **Neural networks based traffic prediction for cell discarding policy**
Lin Hsiou-Ping; Ouyang Yen-Chieh;
Neural Networks,1997., International Conference on , Volume: 4 , 9-12 June 1997
Pages:2051 - 2056 vol.4

[Abstract] [PDF Full-Text (448 KB)] IEEE CNF

---

17 **Predictive signal processing in instrumentation and measurement: A tutorial review**
Ovaska, S.J.;
Instrumentation and Measurement Technology Conference, 1997. IMTC/97. Proceedings. 'Sensing, Processing, Networking'., IEEE , Volume: 1 , 19-21 May 1997
Pages:48 - 53 vol.1

[Abstract] [PDF Full-Text (564 KB)] IEEE CNF

---

18 **Proceedings of the 36th IEEE Conference on Decision and Control**

Decision and Control, 1997., Proceedings of the 36th IEEE Conference on , Volume: 1 , 10-12 Dec. 1997
[Abstract] [PDF Full-Text (4812 KB)] IEEE CNF

---

19 **Combined speech and audio coding using non-linear adaptations**
Cheung-Fat Chan;
Speech Coding For Telecommunications Proceeding, 1997, 1997 IEEE Workshop on , 7-10 Sept. 1997
Pages:105 - 106

[Abstract] [PDF Full-Text (200 KB)] IEEE CNF

20 **Modeling and control of amino acid starvation-induced apoptosis in CHO cell cultures**
Simon, L.; Karim, M.N.;
American Control Conference, 2002. Proceedings of the 2002 , Volume: 2 , 8-10 May 2002
Pages:1579 - 1584 vol.2

[Abstract] [PDF Full-Text (503 KB)] IEEE CNF

21 **Proceedings of the 2001 American Control Conference. (Cat. No.01CH37148)**

American Control Conference, 2001. Proceedings of the 2001 , Volume: 1 , 25-27 June 2001
[Abstract] [PDF Full-Text (3512 KB)] IEEE CNF

22 **Proceedings of the 40th IEEE Conference on Decision and Control (Cat. No.01CH37228)**

Decision and Control, 2001. Proceedings of the 40th IEEE Conference on , Volume: 4 , 4-7 Dec. 2001
[Abstract] [PDF Full-Text (2864 KB)] IEEE CNF

23 **Proceedings of the 38th IEEE Conference on Decision and Control (Cat. No.99CH36304)**

Decision and Control, 1999. Proceedings of the 38th IEEE Conference on , Volume: 1 , 7-10 Dec. 1999
[Abstract] [PDF Full-Text (4048 KB)] IEEE CNF

24 **Proceedings of the 1998 American Control Conference. ACC (IEEE Cat. No.98CH36207)**

American Control Conference, 1998. Proceedings of the 1998 , Volume: 1 , 24-26 June 1998
[Abstract] [PDF Full-Text (3072 KB)] IEEE CNF

25 **Growing filters for finite impulse response networks**
Diepenhorst, M.; Nijhuis, J.A.G.; Venema, R.S.; Spaanenburg, L.;
Neural Networks, 1995. Proceedings., IEEE International Conference on , Volume: 2 , 27 Nov.-1 Dec. 1995
Pages:854 - 859 vol.2

[Abstract] [PDF Full-Text (588 KB)] IEEE CNF

26 **Single channel adaptive noise cancelation for enhancing noisy speech**
Hae Dong Gahng; Keun Sung Bae;
Speech, Image Processing and Neural Networks, 1994. Proceedings, ISSIPNN '94., 1994 International Symposium on , 13-16 April 1994
Pages:343 - 346 vol.1

[Abstract] [PDF Full-Text (212 KB)] IEEE CNF

27 **Dynamic bandwidth allocation for efficient transport of real-time VBR video over ATM**
Chong, S.; Li, S.-Q.; Ghosh, J.;
INFOCOM '94. Networking for Global Communications. 13th Proceedings IEEE , 12-16 June 1994
Pages:81 - 90 vol.1

[Abstract] [PDF Full-Text (900 KB)] IEEE CNF

28 **Non-linear short-term prediction in speech coding**
Thyssen, J.; Nielsen, H.; Hansen, S.D.;
Acoustics, Speech, and Signal Processing, 1994. ICASSP-94., 1994 IEEE International Conference on , Volume: i , 19-22 April 1994
Pages:I/185 - I/188 vol.1

[Abstract] [PDF Full-Text (220 KB)] IEEE CNF

29 **Prediction-based networks with ECG application**
Taur, J.S.; Kung, S.Y.;
Neural Networks, 1993., IEEE International Conference on , 28 March-1 April 1993
Pages:1920 - 1925 vol.3

[Abstract] [PDF Full-Text (372 KB)] IEEE CNF

30 **On design and evaluation of tapped-delay neural network architectures**
Svarer, C.; Hansen, L.K.; Larsen, J.;
Neural Networks, 1993., IEEE International Conference on , 28 March-1 April 1993
Pages:46 - 51 vol.1

[Abstract] [PDF Full-Text (392 KB)] IEEE CNF

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---

31 **Noisy speech recognition via wavelet transform enhancement**
Moon, S.; Hwang, J.-N.;
Signals, Systems and Computers, 1992. 1992 Conference Record of The Twenty-Sixth Asilomar Conference on , 26-28 Oct. 1992
Pages:1086 - 1090 vol.2

[Abstract] [PDF Full-Text (292 KB)] IEEE CNF

---

32 **Using CNLS-net to predict the Mackey-Glass chaotic time series**
Mead, W.C.; Jones, R.D.; Lee, Y.C.; Barnes, C.W.; Flake, G.W.; Lee, L.A.; O'Rourke, M.K.;
Neural Networks, 1991., IJCNN-91-Seattle International Joint Conference on , Volume: ii , 8-14 July 1991
Pages:485 - 490 vol.2

[Abstract] [PDF Full-Text (348 KB)] IEEE CNF

---

33 **On the use of TDNN-extracted features information in talker identification**
Bennani, Y.; Gallinari, P.;
Acoustics, Speech, and Signal Processing, 1991. ICASSP-91., 1991 International Conference on , 14-17 April 1991
Pages:385 - 388 vol.1

[Abstract] [PDF Full-Text (312 KB)] IEEE CNF

---

34 **TDNN-LR continuous speech recognition system using adaptive incremental TDNN training**
Sawai, H.;
Acoustics, Speech, and Signal Processing, 1991. ICASSP-91., 1991 International

Conference on , 14-17 April 1991
Pages:53 - 56 vol.1

[Abstract] [PDF Full-Text (396 KB)] IEEE CNF

---

35 **A neural network implementation of the median filter**
Shi, P.; Ward, R.K.;
Communications, Computers and Signal Processing, 1989. Conference Proceeding., IEEE Pacific Rim Conference on , 1-2 June 1989
Pages:513 - 516

[Abstract] [PDF Full-Text (220 KB)] IEEE CNF

---

36 **An ANN based approach to improve the speed of a differential equation based distance relaying algorithm**
Cho, K.R.; Kang, Y.C.; Kim, S.S.; Park, J.K.; Kang, S.H.; Kim, K.H.;
Power Delivery, IEEE Transactions on , Volume: 14 , Issue: 2 , April 1999
Pages:349 - 357

[Abstract] [PDF Full-Text (644 KB)] IEEE JNL

---

37 **NN-PLS based on-line component soft-analyzer for Tennessee Eastman process**
Wang Hai-qing; Gao Yan-chen; Song Kai;
Intelligent Control and Automation, 2004. WCICA 2004. Fifth World Congress on , Volume: 4 , 15-19 June 2004
Pages:3653 - 3657 Vol.4

[Abstract] [PDF Full-Text (396 KB)] IEEE CNF

---

38 **A modified FIR network for time series prediction**
Ho Joon Kim; Won Don Lee; Hyun Seung Yang;
Neural Information Processing, 2002. ICONIP '02. Proceedings of the 9th International Conference on , Volume: 5 , 18-22 Nov. 2002
Pages:2597 - 2600 vol.5

[Abstract] [PDF Full-Text (412 KB)] IEEE CNF

---

39 **Laser satellite communication: precise estimation of the satellite position and synchronization and the stabilization of the beam on the receiving satellite**
Lee Young Ju; Christian, T.;
National Aerospace and Electronics Conference, 2000. NAECON 2000. Proceedings of the IEEE 2000 , 10-12 Oct. 2000
Pages:696 - 703

[Abstract] [PDF Full-Text (524 KB)] IEEE CNF

---

40 **Reconstruction of chaotic dynamics using a noise-robust embedding method**
Yoshida, W.; Ishii, S.; Sato, M.;
Acoustics, Speech, and Signal Processing, 2000. ICASSP '00. Proceedings. 2000 IEEE International Conference on , Volume: 1 , 5-9 June 2000

Pages:181 - 184 vol.1

[Abstract] [PDF Full-Text (304 KB)] IEEE CNF

---

41 **Neural network tools for stellar light prediction**
Cholewo, T.J.; Zurada, J.M.;
Aerospace Conference, 1997. Proceedings., IEEE , Volume: 3 , 1-8 Feb. 1997
Pages:415 - 422 vol.3

[Abstract] [PDF Full-Text (596 KB)] IEEE CNF

---

42 **Comparisons of artificial neural networks for on-line identification of a nonlinear multivariate electromechanical process**
Kamwa, I.; Martin, S.; Grondin, R.;
Instrumentation and Measurement Technology Conference, 1997. IMTC/97. Proceedings. 'Sensing, Processing, Networking'., IEEE , Volume: 2 , 19-21 May 1997
Pages:1106 - 1111 vol.2

[Abstract] [PDF Full-Text (476 KB)] IEEE CNF

---

43 **Processing of analogy in the thalamocortical circuit**
Choe, Y.;
Neural Networks, 2003. Proceedings of the International Joint Conference on , Volume: 2 , 20-24 July 2003
Pages:1480 - 1485 vol.2

[Abstract] [PDF Full-Text (497 KB)] IEEE CNF

---

44 **Gray-box approach to fault diagnosis of dynamical systems**
Zak, M.; Han Park;
Aerospace Conference, 2001, IEEE Proceedings. , Volume: 2 , 10-17 March 2001
Pages:2/669 - 2/676 vol.2

[Abstract] [PDF Full-Text (552 KB)] IEEE CNF

---

45 **Polynomial predictive filters: complementing technique to fuzzy filtering**
Valiviita, S.; Xiao Zhi Gao; Ovaska, S.J.;
Systems, Man, and Cybernetics, 1998. 1998 IEEE International Conference on , Volume: 5 , 11-14 Oct. 1998
Pages:4648 - 4652 vol.5

[Abstract] [PDF Full-Text (416 KB)] IEEE CNF

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---

46 **Non-linear speech analysis using recurrent radial basis function networks**
Moakes, P.A.; Beet, S.W.;
Neural Networks for Signal Processing [1994] IV. Proceedings of the 1994 IEEE Workshop , 6-8 Sept. 1994
Pages:319 - 328

[Abstract] [PDF Full-Text (400 KB)] IEEE CNF

---

47 **Dispersive networks for nonlinear adaptive filters**
Day, S.P.; Davenport, M.R.; Camporese, D.S.;
Neural Networks for Signal Processing [1992] II., Proceedings of the 1992 IEEE-SP Workshop , 31 Aug.-2 Sept. 1992
Pages:540 - 549

[Abstract] [PDF Full-Text (364 KB)] IEEE CNF

---

48 **Visual motion compensation using a neural shifter circuit**
Olshausen, B.A.;
Systems, Man and Cybernetics, 1990. Conference Proceedings., IEEE International Conference on , 4-7 Nov. 1990
Pages:829 - 831

[Abstract] [PDF Full-Text (232 KB)] IEEE CNF

---

49 **Adaptive receivers for removing linear and nonlinear intersymbol interference by mean of time delay neural nets (AR-TDNN)**
Garcia-Gomez, R.; Gomez-Mena, J.; Diez del Rio, L.;
Acoustics, Speech, and Signal Processing, 1989. ICASSP-89., 1989 International Conference on , 23-26 May 1989

Pages:2368 - 2371 vol.4

[Abstract] [PDF Full-Text (168 KB)] **IEEE CNF**

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1 A survey on wavelet applications in data mining

Tao Li, Qi Li, Shenghuo Zhu, Mitsunori Ogihara

December 2002 **ACM SIGKDD Explorations Newsletter**, Volume 4 Issue 2

Full text available: pdf(330.06 KB) Additional Information: full citation, abstract, references, citings

Recently there has been significant development in the use of wavelet methods in various data mining processes. However, there has been written no comprehensive survey available on the topic. The goal of this is paper to fill the void. First, the paper presents a high-level data-mining framework that reduces the overall process into smaller components. Then applications of wavelets for each component are reviewd. The paper concludes by discussing the impact of wavelets on data mining research an ...

2 Constrained formulations and algorithms for stock-price predictions using recurrent FIR neural networks

Benjamin W. Wah, Minglun Qian

July 2002 **Eighteenth national conference on Artificial intelligence**

Additional Information: full citation, abstract, references, index terms

In this paper, we develop new constrained artificial-neural-network (ANN) formulations and learning algorithms to predict future stock prices, a difficult time-series prediction problem. Specifically, we characterize stock prices as a non-stationary noisy time series, identify its predictable low-frequency components, develop strategies to predict missing low-frequency information in the lag period of a filtered time series, model the prediction problem by a recurrent FIR ANN, formulate the trai ...

3 Dynamic model abstraction

Kangsun Lee, Paul A. Fishwick

November 1996 **Proceedings of the 28th conference on Winter simulation**

Full text available: pdf(821.69 KB) Additional Information: full citation, references, citings

4 Real time application of artificial neural network for incipient fault detection of induction machines

Mo-yuen Chow, Sui Oi Yee

June 1990 **Proceedings of the third international conference on Industrial and**

engineering applications of artificial intelligence and expert systems - Volume 2

Full text available: pdf(751.83 KB) Additional Information: full citation, abstract, references, index terms

This paper describes several artificial neural network architectures for real time application in incipient fault detection of induction machines. The artificial neural networks perform the fault detection in real time, based on direct measurements from the motor, and no rigorous mathematical model of the motor is needed. Different approaches used to develop a reliable fault detector are presented and compared in this paper. The designed networks vary in complexity and accuracy. A high-orde ...

5 Time series forecasting using neural networks

Thomas Kolarik, Gottfried Rudorfer

August 1994 **ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL : the language and its applications: the language and its applications**, Volume 25 Issue 1

Full text available: pdf(657.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Artificial neural networks are suitable for many tasks in pattern recognition and machine learning. In this paper we present an APL system for forecasting univariate time series with artificial neural networks. Unlike conventional techniques for time series analysis, an artificial neural network needs little information about the time series data and can be applied to a broad range of problems. However, the problem of network "tuning" remains: parameters of the backpropagation a ...

6 A measurement-based admission control algorithm for integrated service packet networks

Sugih Jamin, Peter B. Danzig, Scott J. Shenker, Lixia Zhang

February 1997 **IEEE/ACM Transactions on Networking (TON)**, Volume 5 Issue 1

Full text available: pdf(284.33 KB) Additional Information: full citation, references, citings, index terms

Keywords: predictive service, quality-ofservice guarantee, real-time traffic

7 Query evaluation techniques for large databases

Goetz Graefe

June 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 2

Full text available: pdf(9.37 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Database management systems will continue to manage large data volumes. Thus, efficient algorithms for accessing and manipulating large sets and sequences will be required to provide acceptable performance. The advent of object-oriented and extensible database systems will not solve this problem. On the contrary, modern data models exacerbate the problem: In order to manipulate large sets of complex objects as efficiently as today's database systems manipulate simple records, query-processi ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, extensible database systems, iterators, object-oriented database systems, operator model of parallelization, parallel algorithms, relational database systems, set-matching algorithms, sort-hash duality

8 Parallelization and analysis of a linear adaptive filtering algorithm

Richard K. Acree, David T. Croley, Nasr Ullah, Mario J. Gonzalez, Darioush M. Samani
March 1993 **Proceedings of the 1993 ACM/SIGAPP symposium on Applied computing: states of the art and practice**
Full text available: pdf(848.40 KB) Additional Information: full citation, references, index terms

9 Interconnect noise avoidance methodologies & slew rate prediction: Interconnect and noise immunity design for the Pentium 4 processor
Rajesh Kumar
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(407.27 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the key challenges, design methods, CAD and learnings in the area of interconnect and noise immunity design for the Intel Pentium 4 processor.This high frequency (currently at 3 Ghz with 6 Ghz execution core) design required aggressive domino, pulsed and other novel high speed circuit families that are very noise sensitive. Controlling interconnect delay, capacitive and inductive coupling is of paramount importance at such high frequencies and edge rates, made more difficult ...

10 Research sessions: moving objects: Prediction and indexing of moving objects with unknown motion patterns
Yufei Tao, Christos Faloutsos, Dimitris Papadias, Bin Liu
June 2004 **Proceedings of the 2004 ACM SIGMOD international conference on Management of data**
Full text available: pdf(335.08 KB) Additional Information: full citation, abstract, references

Existing methods for peediction spatio-temporal databases assume that objects move according to linear functions. This severely limits their applicability, since in practice movement is more complex, and individual objects may follow drastically diffferent motion patterns. In order to overcome these problems, we first introduce a general framework for monitoring and indexing moving objects, where (i) each boject computes individually the function that accurately captures its movement and (ii) a ...

11 Chaos engineering in Japan
Kazuyuki Aihara, Ryu Katayama
November 1995 **Communications of the ACM**, Volume 38 Issue 11
Full text available: pdf(431.25 KB) Additional Information: full citation, abstract, references, index terms

Since deterministic chaos is not only a profound concept in science but also a ubiquitous phenomenon in real-world nonlinear systems, extending to a variety of temporal and spatial scales, it can be naturally related to applications in science and technology [4]. In fact, it is not difficult to find the buds of such possible applications in historical papers by Van der Pol and Van der Mark [22], Ulam and von Neumann [21], and Kalman [12], although the term deterministic chaos

12 Detecting Chaos in the Field
Juergen Kahrs
July 2000 **Linux Journal**
Full text available: html(16.73 KB) Additional Information: full citation, abstract, references, index terms

All that is real is reasonable, and all that is reasonable is real. -- G.W.F. Hegel, 1770-1831

13 Poster session: Implementation of digital fixed-point approximations to continuous-time IIR filters
J. E. Carletta, R. J. Veillette, F. W. Krach, Z. Fang

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

An analytical framework for the implementation of digital infinite impulse response filters in fixed-point hardware on FPGAs is presented. It presumes that a continuous-time filter with the desired response is given. Within the framework, the constant coefficient bit widths are determined by accounting for the sensitivity of the filter's pole and zero locations with respect to the coefficient perturbations. The internal signal bit widths are determined by calculating theoretical bounds on the ra ...

14 Poster session: Recursive circuit clustering for minimum delay and area

Mehrdad Eslami Dehkordi, Stephen D. Brown

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

We present an effective recursive algorithm for circuit clustering for delay and area minimization, which is applicable to FPGAs. At the highest level of clustering, the circuit is clustered using a modified single-level clustering algorithm. A cluster to netlist transformation technique is proposed, which converts each cluster into a new subcircuit. The algorithm then continues recursively by clustering the generated subcircuits into further levels of clusters. To reduce the amount of node dupl ...

15 Poster session: Lattice adaptive filter implementation for FPGA

Zdenek Pohl, Rudolf Matoušek, Jirí Kadlec, Milan Tichý, Miroslav Lícko

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Our poster introduces an innovative RLS Lattice filter implementation for FPGAs. The signal processing applications typically require wide numeric range, and that poses a problem when using an FPGA implementation. Our approach is based on arithmetic using logarithmic numeric representation (LNS). The test application - an adaptive noise canceller - has been optimized for the Xilinx Virtex devices. It consumes roughly 70% of all logic resources of the XCV800 device and all block memory cells. The ...

16 A framework for bandwidth management in ATM networks—aggregate equivalent bandwidth estimation approach

Zbigniew Dziong, Marek Juda, Lorne G. Mason

February 1997 **IEEE/ACM Transactions on Networking (TON)**, Volume 5 Issue 1

Full text available: pdf(359.92 KB) Additional Information: full citation, references, citings, index terms

17 Emerging design and tool challenges in RF and wireless applications: New techniques for non-linear behavioral modeling of microwave/RF ICs from simulation and nonlinear microwave measurements

David E. Root, John Wood, Nick Tufillaro

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(337.31 KB) Additional Information: full citation, abstract, references, index terms

This paper compares and contrasts recent nonlinear behavioral modeling techniques designed for microwave and RFIC applications which arise in radio and communication systems, and in the design of broad-band nonlinear components used for microwave instrumentation. These techniques include dynamic neural networks and nonlinear time

series models in the time-domain, nonlinear describing functions in the frequency domain, and envelope-based methods in mixed time and frequency domains. Approaches to ...

Keywords: MMICs, RFICs, behavioral modeling, circuit simulation, nonlinear dynamics, nonlinear modeling, nonlinear simulation

18 Learning evaluation functions to improve optimization by local search

Justin Boyan, Andrew W. Moore

September 2001 **The Journal of Machine Learning Research**, Volume 1

Full text available: pdf(643.21 KB) Additional Information: full citation, abstract

This paper describes algorithms that learn to improve search performance on large-scale optimization tasks. The main algorithm, STAGE, works by learning an evaluation function that predicts the outcome of a local search algorithm, such as hillclimbing or Walksat, from features of states visited during search. The learned evaluation function is then used to bias future search trajectories toward better optima on the same problem. Another algorithm, X-STAGE, transfers previously learned evaluation ...

19 Poster session: On hiding latency in reconfigurable systems: the case of merge-sort for an FPGA-based system

Hossam ElGindy, George Ferizis

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Recursive solutions are effective software techniques that are difficult to map into hardware due to their dependency on input size and data values. As a result, most high-level design tools do not allow for recursive calls. In this paper we present a technique for mapping the merge-sort algorithm, as a case study, into a reconfigurable system. Our mapping employs an on-line prediction method to reconfigure the necessary hardware only when the need arises, and to hide the reconfiguration delay. ...

20 Poster session: Design framework for the implementation of the 2-D orthogonal discrete wavelet transform on FPGA

A. Benkrid, D. Crookes, K. Benkrid

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This paper gives a design framework for the implementation of the 2-D Orthogonal Discrete Wavelet Transform (DWT) on FPGA. The architecture is based on the Pyramid Algorithm Analysis. Our architecture spatially maps the multistage filter banks of the DWT onto the Xilinx Virtex-E FPGA family. In this paper we propose a novel FIR structure to handle the computation along the borders using symmetric extension. The paper includes a new detailed mathematical approach to determine the architecture's d ...

Terms used **delay** and **filter** and **nonlinear approximator** or **artificial neural** and **predict** or **forecast**

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Relevance scale

21 Technical reports

SIGACT News Staff

January 1980 **ACM SIGACT News**, Volume 12 Issue 1

Full text available: pdf(5.28 MB) Additional Information: full citation

22 Poster session: A SC-based novel configurable analog cell

Binlin Guo, Jiarong Tong

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This paper presents a high performance Configurable Analog Cell (CAC) which is made up of a Basic Configurable Analog Cell (BCAC) and a digital converter block. The CAC can be used either for Field Programmable Analog Array (FPAA) or for Field Programmable Digital-Analog Mixed Array (FPMA). The BCAC include three innovative Programmable Switch Blocks (PSBs), three Programmable Capacitor Arrays (PCAs), and an amplifier. PSB and PCA can be programmed to generate many equivalent components. In addi ...

23 Poster session: A physical retiming algorithm for field programmable gate arrays

Peter Suaris, Dongsheng Wang, Pei-Ning Guo, Nan-Chi Chou

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In this paper, we present a physical retiming algorithm for sequential circuits implemented in field programmable gate arrays (FPGAs). This algorithm can speed up the sequential circuits by reducing delay of all critical paths with negative slacks. By taking advantage of the physical information provided by placed circuits, this algorithm integrates two operations: retiming and register duplication. Retiming moves registers across combinational components. Register duplication moves registers ac ...

24 Poster session: FPGA-based design of an evolutionary controller for collision-free robot navigation

M. A. H. B. Azhar, K. R. Dimond

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium**

on Field programmable gate arrays

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The employment of field programmable gate arrays (FPGAs) to a robot controller is very attractive, since it allows for fast IC prototyping and low cost modifications. The speedup is achieved because of pipelining and dedicated functions in hardware that are customized to the problem. The self learning ability and the adaptive nature of an Artificial Neural Network (ANN) makes it a good candidate for the control structure of a robot's navigation. An evolutionary approach in designing robots can e ...

25 Poster session: Design of a fingerprint system using a hardware/software environment

Lee Vanderlei Bonato, Rolf Fredi Molz, João Carlos Furtado, Marcos Flores Ferrão, Fernando G. Moraes

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Processing system of fingerprint are CPU time intensive, being normally implemented in software. This paper present a new algorithm for fingerprint features localization, that can be easily implemented in hardware (system-on-a-chip, FPGA). This algorithm is composed by 3 stages, first stage read a fingerprint image (255x255pixels, ash tones) and apply a Gaussian Filter, after this, apply a absolute difference mask (ADM) for detector the edges in the image filtered and the last stage look for fin ...

26 Poster session: A four-bit full adder implemented on fast SiGe FPGAs with novel power control scheme

K. Zhou, M. Chu, C. You, J.-R. Guo, Channakeshav, J. Mayega, B. S. Goda, R. P. Kraft, J. F. McDonald

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The low operating speed of current CMOS Field Programmable Gate Arrays (FPGAs), i.e., 10-220 MHz, has prevented their use in high-speed digital applications. With the advent of IBM Silicon Germanium (SiGe) 7HP technology, designers have been able to design FPGAs operating in the gigahertz range. This paper is going to elaborate on the implementation of a 4-bit ripple-carry full adder (FA) on the new SiGe FPGA with new architectures and a novel power management strategy. The 1-bit FA can be reali ...

27 Poster session: Synthetic circuit generation using clustering and iteration

Paul D. Kundarewich, Jonathan Rose

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The development of next-generation CAD tools and FPGA architectures requires benchmark circuits to experiment with new algorithms and architectures. There has always been a shortage of good public benchmarks for these purposes, and even companies that have access to proprietary customer designs could benefit from designs that meet size and other particular specifications. In this paper, we present a new method of generating realistic synthetic benchmark circuits to help alleviate this shortage. ...

28 Poster session: An estimation and exploration methodology from system-level specifications: application to FPGAs

Sebastien Bilavarn, Guy Gogniat, Jean Luc Philippe

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Rapid evaluation and design space exploration from early specifications are important issues in the design cycle. We propose an original area vs. delay estimation methodology that targets reconfigurable architectures. Two main steps compose the estimation flow: i) structural estimations where architectural solutions are defined at the RT level, this step is technological independent and performs an automatic design space exploration and ii) physical estimations which perform technology mapping t ...

29 Poster session: A high resolution diagnosis technique for open and short defects in FPGA interconnects

Mehdi Baradaran Tahoori

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

A two-step diagnosis flow, coarse-grain and fine-grain, is presented in order to identify a faulty element in the FPGA interconnects. The fault models used for interconnect are open, resistive-open, and bridging fault. The coarse-grain phase identifies the faulty net, the routing between two consecutive sequential elements in the FPGA. This phase is performed by just post-processing tester results for the test configurations used for interconnect testing. During the fine-grain step, the faulty n ...

30 Poster session: Application-dependent testing of FPGAs for bridging faults

Mehdi Baradaran Tahoori

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

A new technique is presented for testing for bridging faults in the interconnects of an arbitrary design implemented in an FPGA. The configuration of the routing resources used in the original design remains unchanged in the test configurations. Only the logic blocks used in the design are reprogrammed in order to implement single-term functions, logic functions with only one minterm or one maxterm. As shown by formal proofs, all activated faults are detected when single-term functions and appro ...

31 Poster session: Design strategies and modified descriptions to optimize cipher FPGA implementations: fast and compact results for DES and triple-DES

Gaël Rouvroy, Francois-Xavier Standaert, Jean-Jacques Quisquater, Jean-Didier Legat

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

We propose a new mathematical DES description that allows optimized implementations. It also provides the best DES and triple-DES FPGA implementations known in term of ratio throughput/area, where area means the number of FPGA slices used. First, we get a less resource consuming unrolled DES implementation that works at data rates of 21.3 Gbps (333 MHz), using VIRTEX II technology. In this design, the plaintext, the key and the mode (encryption/decrytion) can be changed on a cycle-by-cycle basis ...

32 Poster session: Wireless sensor networks: a power-scalable motion estimation IP for hybrid video coding

Federico Quaglio, Maurzio Martina, Fabrizio Vacca, Guido Masera, Andrea Molino, Gianluca Piccinini, Maurizio Zamboni

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Wireless Sensor Networks are an emerging phenomenon in the research community. The design and development of network architectures and nodes implementation are fostering many research activities. Due to their wide application fields and pervasive employment possibilities, the investigation of novel classes of wireless sensor nodes is of great concern. In this paper we presented a novel Power-Scalable Motion Estimation IP suitable for video-surveillance over Wireless Sensor Networks. The proposed ...

33 Poster session: An FPGA architecture with built-in error correction capability

P. K. Lala, B. Kiran Kumar

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The use of very deep submicron technology makes VLSI-based digital systems more susceptible to transient or soft errors, and thus compromises their reliability. This paper proposes an FPGA architecture inspired by the human immune system that allows tolerance of transient errors. The architecture is composed of a two-dimensional array of identical functional cells with different genetic codes. These codes are chosen based on the required functions to be performed by the functional cells. An erro ...

34 Poster session: Reconfigurable randomized K-way graph partitioning

Fatih Kocan

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In this paper, a randomized k-way graph partitioning algorithm is mapped onto reconfigurable hardware. The randomized algorithm relies on repetitive running of the same algorithm with different random number sequences to achieve the (near-)optimal solution. The run-time and hardware requirements of this reconfigurable solution per a random number sequence are O(|V|-K) cycles and O(|V|log|V|+|E|) gates and flip-flops, respectively. Performance is improved further at the expense of more hardware b ...

35 Poster session: An automated and power-aware framework for utilization of IP cores in hardware generated from C descriptions targeting FPGAs

Alex Jones, Prith Banerjee

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Use of hand optimized Intellectual Property (IP) logic cores is prolific in hardware design. While IP cores remain a standard way to utilize the improvement in FPGA technology and contend with time to market pressure through reuse, popularity of tools generating hardware descriptions from high-level languages is also increasing in popularity. PACT HDL combines these two methods within a power-aware framework. The PACT HDL compiler generates power optimized VHDL/Verilog from a C language descript ...

36 Poster session: Power-aware architectures and circuits for FPGA-based signal processing

Frank Honoré, Ben Calhoun, Anantha Chandrakasan

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This work showcases a power-aware system design methodology for DSP applications on

reconfigurable hardware platforms. In particular, an enhanced FPGA architecture is proposed and analyzed for a deep submicron process technology. These enhancements reduce Configurable Logic Block (CLB) usage for distributed arithmetic implementations of signal processing applications by 50% or more thereby reducing the load on interconnect resources. Multi-Threshold CMOS (MTCMOS) circuit design techniques are ag ...

37 Poster session: FPGAs in critical hardware/software systems

Adrian J. Hilton J. Adrian J. Hilton, Gemma Townson, Jon G. Hall

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

FPGAs are being used in increasingly complex roles in critical systems, interacting with conventional critical software. Established safety standards require rigorous justification of safety and correctness of the conventional software in such systems. Newer standards now make similar requirements for safety-related electronic hardware, such as FPGAs, in these systems. In this paper we examine the current state-of-the-art in programming FPGAs, and their use in conventional (low-criticality) hard ...

38 Poster session: On computation and resource management in an FPGA-based computation environment

Soheil Ghiasi, Karlene Nguyen, Elaheh Bozorgzadeh, Majid Sarrafzadeh

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract, citings

The idea of managing the comprising computations of an application executed in an FPGA-based system is presented. An efficient algorithm for exploiting the timing slack of building blocks of the application is proposed. The slack of these blocks can be utilized by replacing them with slower but "cheaper" modules and by assigning the computations to the proper resources. Thus, our approach manages the comprising computations and system resources at the same time. This is performed without comprom ...

39 Poster session: Testing for bit error rate in FPGA communication interfaces

Yongquan Fan, Zeljko Zilic

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

FPGAs have witnessed an increased use of dedicated communication interfaces. With their increased use, it is becoming critical to test and properly characterize all such interfaces. Bit error rate (BER) characteristic is one of the basic measures of the performance of any digital communication system. We propose a scheme for BER testing in FPGAs, which exhibits a few orders of magnitude speedup compared to traditional software simulation methods. In this scheme, we include a novel implementation ...

40 Poster session: Using FPGAs for data and reorganization engines: preliminary results for spatial pointer-based data structures

Pedro C. Diniz, Joonseok Park

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

FPGAs have appealing features such as customizable internal and external bandwidth and the ability to exploit vast amounts of fine-grain instruction-level parallelism. In this paper we explore the applicability of these features in using FPGAs as data search and reorganization engines for performing search and reorganization computations over spatial

pointer-based data structures for which traditional computing platforms perform poorly. The preliminary experiments, for a set of simple spatial qu ...

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41 Poster session: Track placement: orchestrating routing structures to maximize routability

Katherine Compton, Scott Hauck

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The design of a routing channel for an FPGA is a complex process, requiring the careful balance of flexibility with silicon efficiency. With the growing move towards embedding FPGAs into SoC designs, and the opportunity to automatically generate FPGA architectures, this problem becomes even more critical. The design of a routing channel requires determining the number of routing tracks, the length of the wires in those tracks, and the positioning of the breaks on the tracks. This paper focuses o ...

42 Poster session: A high-speed successive erasure BCH decoder architecture

Thomas Buerner

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

A new high speed architecture for a BCH successive erasure decoder is presented. The Berlekamp-Massey based decoder by Sarwate and Shanbhag is extended to handle successive erasures. The critical path in the calculation submodules is increased from Tadd+Tmult to Tadd+Tmult+Tmux. The proposed architecture is implemented exemplary for a BCH(63,45,7) code with up to two erasures on a XILINX Spartan2E300-7. Thus a clock frequency of 95 MHz is reached using 47% of the available slices instead of 105 ...

43 Poster session: Customized regular channel design in FPGAs

Elaheh Bozorgzadeh, Majid Sarrafzadeh

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In this paper, we study the problem of customized regular segmentation design in FPGA routing channels. We propose a deterministic algorithm for segmentation design problem in which each interval is assigned to only one segment (1-Segmentation). We solve the problem of maximum number of incremental track assignment of intervals by mincost network flow technique for 1-Segmentation design. The general K-Segmentation design

problem can also be solved by some modifications in our algorithm. We have ...

44 Poster session: A granularity-based classification model for systems-on-a-chip

Stephan Bingemer, Peter Zipf, Manfred Glesner

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Field-programmable logic has become an increasingly important technology for the design of digital circuits. One interesting point in the field of reconfigurable logic is its classification within the implementation space of other technologies. Such a classification gains importance if FPGA technology becomes an integral part of Systems-on-a-Chip (SoC). The poster discusses an approach to classify technologies based on their granularity. Therefore, a new distinction into homogeneous and heteroge ...

45 Poster session: A single-FPGA implementation of image connected component labelling

K. Benkrid, S. Sukhsawas, D. Crookes, S. Belkacemi

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This paper describes an architecture based on a serial iterative algorithm for Image Connected Component Labelling with a hardware complexity O(N) for an NxN image. The algorithm iteratively scans the input image, performing a recursive non-zero maximum neighbourhood operation. A complete forward pass is followed by an inverse pass in which the image is scanned in reverse order. The process is repeated until no change in the image occurs. The algorithm has been coded in Handel C language and tar ...

46 Poster session: A logic based approach to hardware abstraction

K. Benkrid, S. Belkacemi, D. Crookes

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This paper presents a novel approach to hardware abstraction based on the logic programming language Prolog. This is an attempt to satisfy the dual requirement of abstract hardware design and hardware efficiency. Central to this approach is a hardware description environment called HIDE, which provides more abstract hardware descriptions and compositions than are possible in traditional hardware description languages such as VHDL or Verilog. HIDE enables highly scaleable and parameterised compos ...

47 Poster session: Making area-performance tradeoffs at the high level using the AccelFPGA compiler for FPGAs

P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, R. Anderson

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Applications such as digital cell phones, 3G wireless receivers, and voice over IP, require DSP functions that are typically mapped onto general purpose DSP processors. With the introduction of advanced FPGA architectures which provide built-in DSP support such as the Xilinx Virtex-II, and the Altera Stratix, a new hardware alternative is available for DSP designers. DSP design has traditionally been divided into algorithm development and hardware/software implementation. The majority of DSP alg ...

48 Poster session: FPGA implementation of a fast Hadamard transformer for WCDMA

Sanat Kamal Bahl, Jim Plusquellic

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In code division multiple access (CDMA) systems the base station identifies each user in a cell by unique orthogonal (Walsh) codes. The Walsh codes are generated at the transmitter using a Walsh-Hadamard function. A Fast Hadamard Transformer (FHT) is used at the receiver to decode the transmitted codes. The purpose of this study is to design a FHT which utilizes less hardware resources as compared to the existing designs and also suggest means for reducing the input length of the Walsh sequence. ...

49 Industry track papers: Mining heterogeneous gene expression data with time lagged recurrent neural networks

Yulan Liang, Arpad Kelemen

July 2002 **Proceedings of the eighth ACM SIGKDD international conference on Knowledge discovery and data mining**

Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, index terms

Heterogeneous types of gene expressions may provide a better insight into the biological role of gene interaction with the environment, disease development and drug effect at the molecular level. In this paper for both exploring and prediction purposes a Time Lagged Recurrent Neural Network with trajectory learning is proposed for identifying and classifying the gene functional patterns from the heterogeneous nonlinear time series microarray experiments. The proposed procedures identify gene fun ...

Keywords: backpropagation through time, gene expression, heterogeneous, time lagged neural network, trajectory learning

50 MOS circuit models in Network C

William S. Beckett

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Full text available: pdf(684.46 KB) Additional Information: full citation, abstract, references, citings, index terms

Network C is a programming language designed for constructing simulation models of VLSI circuits and systems. The language, which is a superset of C, supports a range of modeling capabilities including approximate solution of Kirchoff equations at the circuit level and discrete event functional simulation at the system level. When used to model a MOS circuit, the system first decomposes the circuit into a set of independent stages. The values of nodes, represented by piece-wise linear funct ...

51 Towards nanocomputer architecture

Paul Beckett, Andrew Jennings

January 2002 **Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture - Volume 6**, Volume 24 Issue 3

Full text available: pdf(1.24 MB) Additional Information: full citation, abstract, references, index terms

At the nanometer scale, the focus of micro-architecture will move from processing to communication. Most general computer architectures to date have been based on a "stored program" paradigm that differentiates between memory and processing and relies on communication over busses and other (relatively) long distance mechanisms. Nanometer-scale electronics --- nanoelectronics - promises to fundamentally change the ground-rules. Processing will be cheap and plentiful, interconnection expensive but ...

Keywords: MIMD, QCA, SIMD, array architecture, computer architecture, device scaling, future trends, micro-architecture, nanocomputer architecture, nanoelectronic technology

52 IFIP Congress-62, Munich, Germany, August 27-September 1, 1962: Abstracts of papers

June 1962 **Communications of the ACM**, Volume 5 Issue 6

Full text available: pdf(1.35 MB) Additional Information: full citation

53 The FINITE STRING Newsletter: Abstracts of current literature

Computational Linguistics Staff

January 1987 **Computational Linguistics**, Volume 13 Issue 1-2

Full text available: pdf(6.15 MB) Additional Information: full citation

Publisher Site

54 Recipes for adjoint code construction

Ralf Giering, Thomas Kaminski

December 1998 **ACM Transactions on Mathematical Software (TOMS)**, Volume 24 Issue 4

Full text available: pdf(301.79 KB) Additional Information: full citation, abstract, references, citings, index terms

Adjoint models are increasingly being developed for use in meteorology and oceanography. Typical applications are data assimilation, model tuning, sensitivity analysis, and determination of singular vectors. The adjoint model computes the gradient of a cost function with respect to control variables. Generation of adjoint code may be seen as the special case of differentiation of algorithms in reverse mode, where the dependent function is a scalar. The described method for adjoint code gene ...

Keywords: adjoint model, adjoint operator, automatic differentiation, computational differentiation, data assimilation, differentiation of algorithms, implicit functions, inverse modeling, optimization, reverse mode

55 Using adaptive linear prediction to support real-time VBR video under RCBR network service model

Abdelnaser Mohammad Adas

October 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 5

Full text available: pdf(229.90 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATM, QoS, VBR, adaptive linear prediction, congestion control

56 Introductory tutorials: Simulation-based optimization: practical introduction to simulation optimization

Jay April, Fred Glover, James P. Kelly, Manuel Laguna

December 2003 **Proceedings of the 35th conference on Winter simulation: driving innovation**

Full text available: Additional Information:

pdf(384.39 KB) full citation, abstract, references

The merging of optimization and simulation technologies has seen a rapid growth in recent years. A Google search on "Simulation Optimization" returns more than six thousand pages where this phrase appears. The content of these pages ranges from articles, conference presentations and books to software, sponsored work and consultancy. This is an area that has sparked as much interest in the academic world as in practical settings. In this paper, we first summarize some of the most relevant appr ...

57 Temporal sequence learning and data reduction for anomaly detection

Terran Lane, Carla E. Brodley

August 1999 **ACM Transactions on Information and System Security (TISSEC)**, Volume 2 Issue 3

Full text available: pdf(628.31 KB) Additional Information: full citation, abstract, references, citings, index terms

The anomaly-detection problem can be formulated as one of learning to characterize the behaviors of an individual, system, or network in terms of temporal sequences of discrete data. We present an approach on the basis of instance-based learning (IBL) techniques. To cast the anomaly-detection task in an IBL framework, we employ an approach that transforms temporal sequences of discrete, unordered observations into a metric space via a similarity measure that encodes intra-attribute depende ...

Keywords: anomaly detection, clustering, data reduction, empirical evaluation, instance based learning, machine learning, user profiling

58 Double exponential smoothing: an alternative to Kalman filter-based predictive tracking

Joseph J. LaViola

May 2003 **Proceedings of the workshop on Virtual environments 2003**

Full text available: pdf(229.71 KB) Additional Information: full citation, abstract, references, index terms

We present novel algorithms for predictive tracking of user position and orientation based on double exponential smoothing. These algorithms, when compared against Kalman and extended Kalman filter-based predictors with derivative free measurement models, run approximately 135 times faster with equivalent prediction performance and simpler implementations. This paper describes these algorithms in detail along with the Kalman and extended Kalman Filter predictors tested against. In addition, we d ...

59 Associative and Parallel Processors

Kenneth J. Thurber, Leon D. Wald

December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4

Full text available: pdf(2.62 MB) Additional Information: full citation, references, citings, index terms

60 Automatic aircraft conflict resolution using genetic algorithms

Nicolas Durand, Jean-Marc Alliot, Joseph Noailles

February 1996 **Proceedings of the 1996 ACM symposium on Applied Computing**

Full text available: pdf(919.64 KB) Additional Information: full citation, references, index terms

Keywords: air traffic control, conflict resolution, genetic algorithms

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(((delay AND filter) AND ("nonlinear approximator" OR "artificial neural")) AND (predict OR forecast)): 76 patents.
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1	6,823,244	Vehicle part control system including electronic sensors
2	6,802,046	Time domain measurement systems and methods
3	6,768,944	Method and system for controlling a vehicle
4	6,757,602	System for determining the occupancy state of a seat in a vehicle and controlling a component based thereon
5	6,757,579	Kalman filter state estimation for a manufacturing system
6	6,751,602	Neural net controller for noise and vibration reduction
7	6,743,167	Method and system for predicting human cognitive performance using data from an actigraph
8	6,740,032	Method and system for predicting human congnitive performance
9	6,738,697	Telematics system for vehicle diagnostics
10	6,738,682	Method and apparatus for scheduling based on state estimation uncertainties
11	6,735,500	Method, system, and computer program product for tactile cueing flight control
12	6,733,036	Automotive electronic safety network
13	6,720,920	Method and arrangement for communicating between vehicles
14	6,704,691	Method and system for in-line monitoring process performance using measurable equipment signals
15	6,697,657	Method and devices for laser induced fluorescence attenuation spectroscopy (LIFAS)
16	6,650,779	Method and apparatus for analyzing an image to detect and identify patterns
17	6,648,367	Integrated occupant protection system
18	6,625,569	Real-time spatio-temporal coherence estimation for autonomous mode identification and invariance tracking

19 6,625,484 Signal evaluation method for detecting QRS complexes in electrocardiogram signals
20 6,601,051 Neural systems with range reducers and/or extenders
21 6,574,754 Self-monitoring storage device using neural networks
22 6,574,501 Assessing blood brain barrier dynamics or identifying or measuring selected substances or toxins in a subject by analyzing Raman spectrum signals of selected regions in the eye
23 6,553,252 Method and system for predicting human cognitive performance
24 6,549,804 System for the prediction, rapid detection, warning, prevention or control of changes in activity states in the brain of a subject
25 6,539,354 Methods and devices for producing and using synthetic visual speech based on natural coarticulation
26 6,535,785 System and method for monitoring and controlling gas plasma processes
27 6,533,316 Automotive electronic safety network
28 6,529,809 Method of developing a system for identifying the presence and orientation of an object in a vehicle
29 6,527,715 System and method for predicting human cognitive performance using data from an actigraph
30 6,526,352 Method and arrangement for mapping a road
31 6,517,107 Methods for controlling a system in a vehicle using a transmitting/receiving transducer and/or while compensating for thermal gradients
32 6,484,133 Sensor response rate accelerator
33 6,459,973 Arrangements for detecting the presence or location of an object in a vehicle and for controlling deployment of a safety restraint
34 6,453,206 Neural network for predicting values in non-linear functional mappings
35 6,452,870 Methods for controlling deployment of an occupant restraint in a vehicle and determining whether the occupant is a child seat
36 6,445,988 System for determining the occupancy state of a seat in a vehicle and controlling a component based thereon
37 6,419,629 Method for predicting human cognitive performance
38 6,418,424 Ergonomic man-machine interface incorporating adaptive pattern recognition based control system
39 6,416,480 Method and apparatus for automated acquisition of the glasgow coma score (AGCS)
40 6,411,946 Route optimization and traffic management in an ATM network using neural computing
41 6,408,227 System and method for controlling effluents in treatment systems
42 6,405,132 Accident avoidance system
43 6,403,384 Device and method for analyzing a biologic sample
44 6,397,136 System for determining the occupancy state of a seat in a vehicle
45 6,377,545 Open loop adaptive access control of ATM networks using a neural network
46 6,370,430 Apparatus and method for controlling the delivery of non-excitatory cardiac contractility modulating signals to a heart
47 6,351,683 System and method for monitoring and controlling gas plasma processes
48 6,301,370 Face recognition from video images
49 6,279,946 Methods for controlling a system in a vehicle using a transmitting/receiving transducer and/or while compensating for thermal gradients
○ 50 6,278,962 Hybrid linear-neural network process control

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(((delay AND filter) AND ("nonlinear approximator" OR "artificial neural")) AND (predict OR forecast)): 76 patents.
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	PAT. NO.	Title
51	6,249,252	Wireless location using multiple location estimators
52	6,241,686	System and method for predicting human cognitive performance using data from an actigraph
53	6,208,963	Method and apparatus for signal classification using a multilayer network
54	6,124,597	Method and devices for laser induced fluorescence attenuation spectroscopy
55	6,024,705	Automated seismic detection of myocardial ischemia and related measurement of cardiac output parameters
56	5,995,868	System for the prediction, rapid detection, warning, prevention, or control of changes in activity states in the brain of a subject
57	5,992,383	Control unit having a disturbance predictor, a system controlled by such a control unit, an electrical actuator controlled by such a control unit, and throttle device provided with such an actuator
58	5,987,444	Robust neutral systems
59	5,920,477	Human factored interface incorporating adaptive pattern recognition based controller apparatus
60	5,904,202	Device for early detection of run-out in continuous casting
61	5,877,954	Hybrid linear-neural network process control
62	5,875,108	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system
63	5,857,978	Epileptic seizure prediction by non-linear methods
64	5,812,992	Method and system for training a neural network with adaptive weight updating and adaptive pruning in principal component space
65	5,774,831	System for improving average accuracy of signals from global positioning system by using a neural network to obtain signal correction values
66	5,774,357	Human factored interface incorporating adaptive pattern recognition based controller apparatus

67 5,743,860 Apparatus and method for epileptic seizure detection using non-linear techniques
68 5,742,694 Noise reduction filter
69 5,732,382 Method for identifying misfire events of an internal combustion engine
70 5,715,372 Method and apparatus for characterizing an input signal
71 5,652,770 Sampled-data filter with low delay
72 5,649,061 Device and method for estimating a mental decision
73 5,555,495 Method for adaptive control of human-machine systems employing disturbance response
74 5,461,559 Hierarchical control system for molecular beam epitaxy
75 5,255,348 Neural network for learning, recognition and recall of pattern sequences
76 4,906,940 Process and apparatus for the automatic detection and extraction of features in images and displays

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